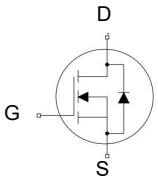
40V N-Channel Power SpeedFET

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Product Summary



V_{DS}= 40V

$R_{DS(ON)}$ = 0.7mΩ

I_D= 325A

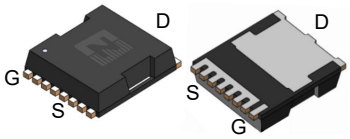
● Features

■AEC-Q101 Qualified

■Low $R_{DS(ON)}$ to minimize conductive loss

■Low Gate Charge for fast switching

■Low Thermal resistance



TOLL

●Application

■BLDC Motor driver

■DC-DC

■Battery protection

●Ordering Information:

Part NO.	ZMSA006N04HR
Marking	ZMS006N04H
Packing Information	REEL TAPE
Basic ordering unit (pcs)	2000

●Absolute Maximum Ratings (T_C=25℃)

Parameter	Symbol	Conditions	Value	Unit
Drain-Source Voltage	V_{DS}		40	V
Gate-Source Voltage①	V_{GS}		±20	V
Continuous Drain Current	I_D	T_C=25℃	325	A
	I_D	T_C=75℃	313	A
	I_D	T_C=100℃	271	A
Pulsed Drain Current	I_{DM}	Pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C;	975	A
Total Power Dissipation	P_D	T_C=25℃	250	W
Total Power Dissipation	P_D	T_A=25℃	5.0	W
Operating Junction Temperature	T_J		-55 to +175	℃
Storage Temperature	T_{STG}		-55 to +175	℃
Single Pulse Avalanche Energy	E_{AS}	L=0.1mH, V_{GS}=10V, Rg=25Ω,	360	mJ
		L=0.5mH, V_{GS}=10V, Rg=25Ω,	680	mJ
ESD Level (HBM)	CLASS 2			

●Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}		-	0.6	°C/W
Thermal resistance, junction-ambient	R_{thJA} ②		-	30	°C/W
Soldering temperature	Tsold		-	260	°C

●Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} =0V, I_D =250uA	40			V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} =V_{DS}, I_D =250uA	2	2.7	4	V
Drain-Source Leakage Current	I_{DSS}	V_{GS}=0V, V_{DS}= 40V			1.0	uA
Gate- Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS} = 0V			100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D= 40A		0.7	0.9	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5V, I_{SD} = 10A		30		s
Diode Forward Voltage	V_{FSD}	V_{GS} =0V, I_{SD} = 40A			1.3	V

●Dynamic characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	Ciss	f = 1MHz, V_{DS}=25V	-	6900	-	pF
Output capacitance	Coss		-	2100	-	
Reverse transfer capacitance	Crss		-	86	-	
Gate Risistance	Rg	f = 1MHz	-	1.4		Ω
Total gate charge	Qg	V_{DD}=15V, I_D=20A, V_{GS}=10V	-	94	-	nC
Gate - Source charge	Qgs		-	21	-	
Gate - Drain charge	Qgd		-	26	-	
Turn-ON Delay time	$t_{D(on)}$	V_{GS}=10V,V_{DS}=15V, R_G =3.3Ω, I_D =20A	-	39	-	ns
Turn-ON Rise time	t_r		-	42	-	ns
Turn-Off Delay time	$t_{D(off)}$		-	31	-	ns
Turn-Off Fall time	t_f		-	12	-	ns
Reverse Recovery Time	t_{RR}	V_{DD}=20V, dI_S/dt = 100A/us, I_S=50A	-	72	-	ns
Reverse Recovery Charge	Q_{RR}		-	85	-	nC

Fig.1 Gate-Charge Characteristics

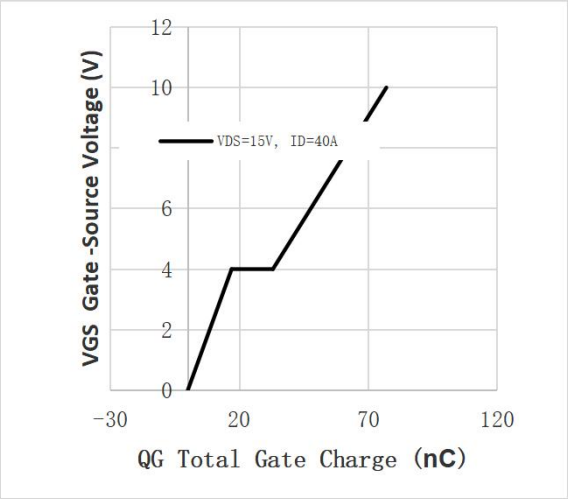


Fig.2 Capacitance Characteristics

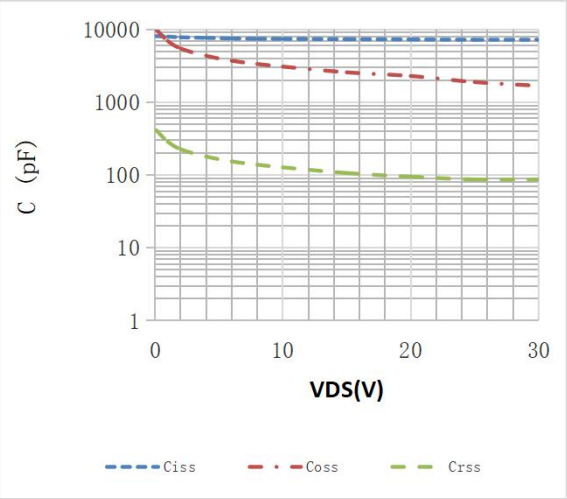


Fig.3 Power Dissipation

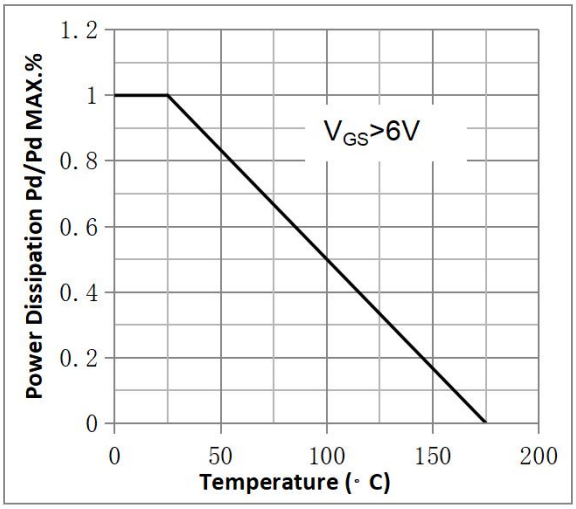


Fig.4 Typical output Characteristics

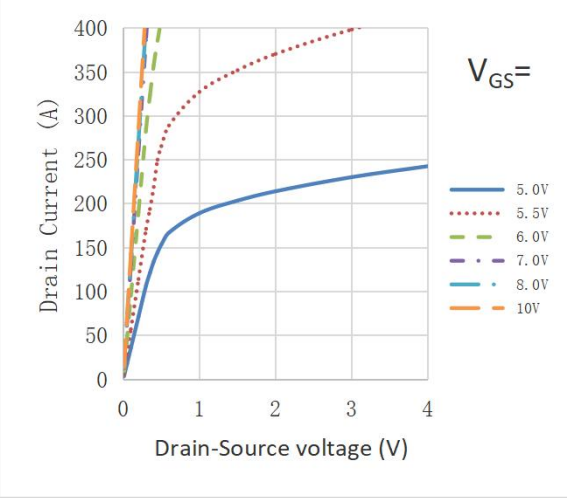


Fig.5 Threshold Voltage V.S Junction Temperature

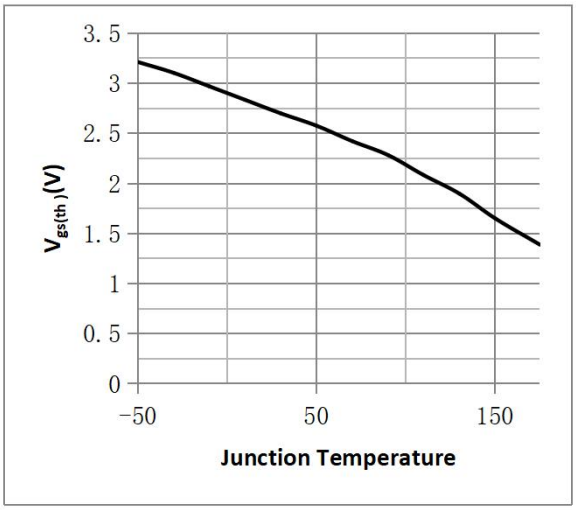


Fig.6 Resistance V.S Drain Current

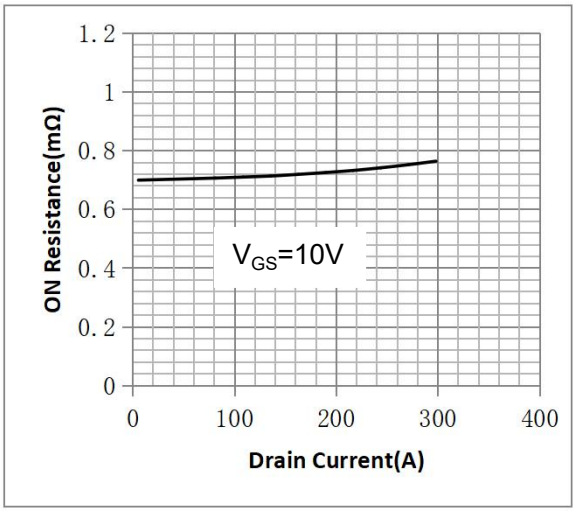


Fig.7 On-Resistance VS Gate Source Voltage

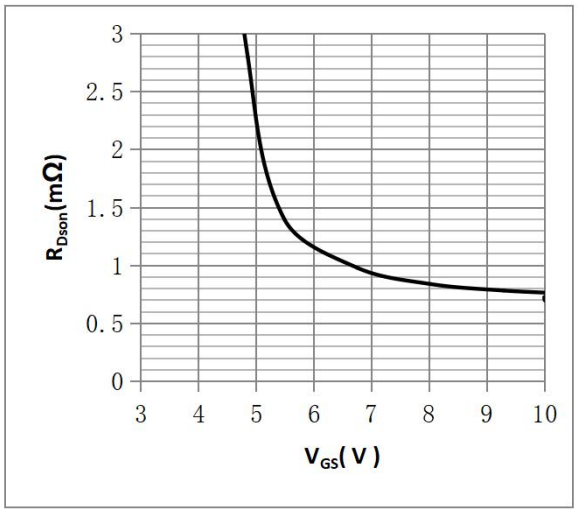


Fig.8 On-Resistance V.S Junction Temperature

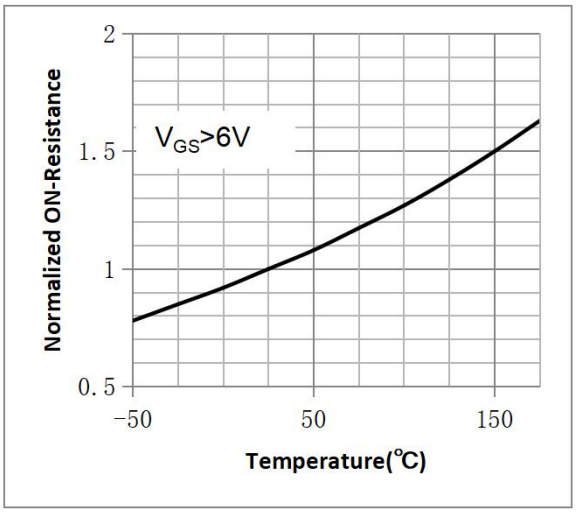


Figure 9. Diode Forward Voltage vs. Current

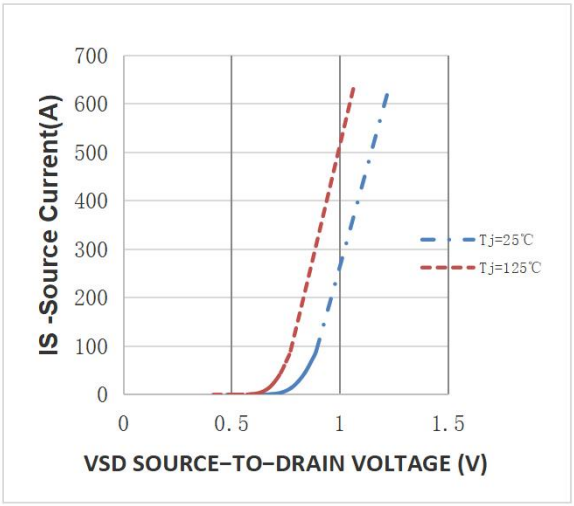


Figure 10. Transfer Characteristics

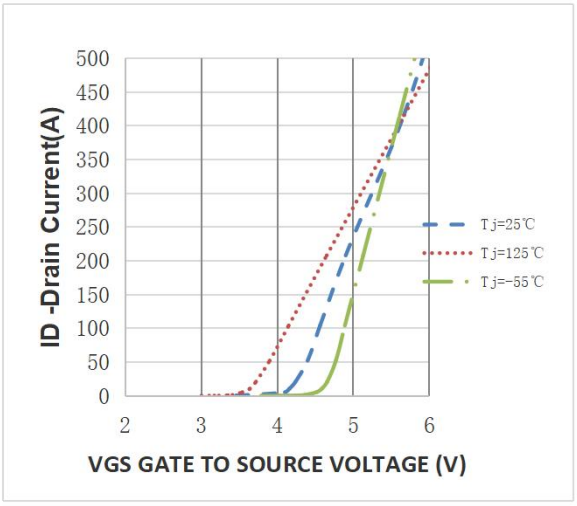


Fig.11 Safe Operating Area

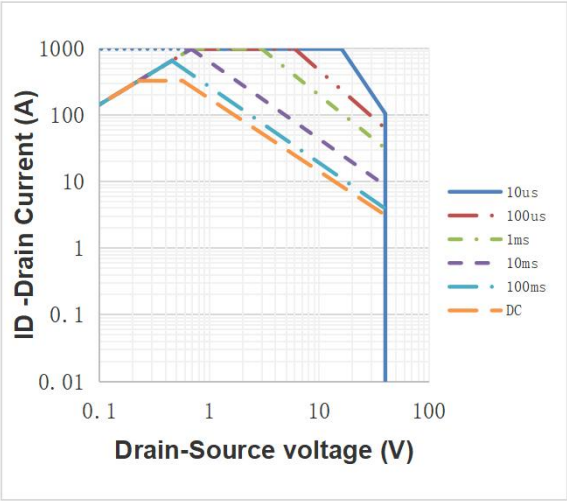
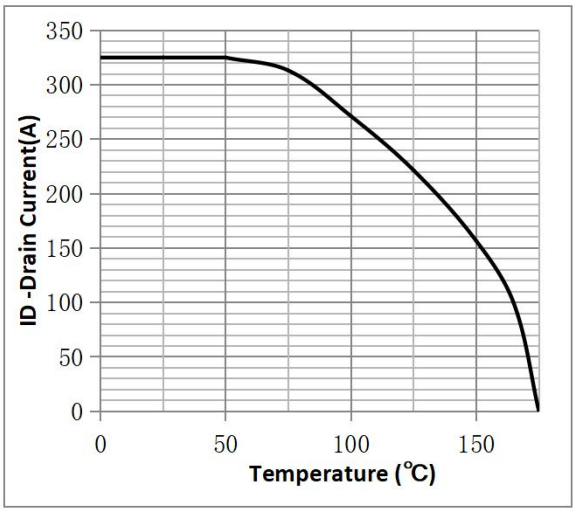
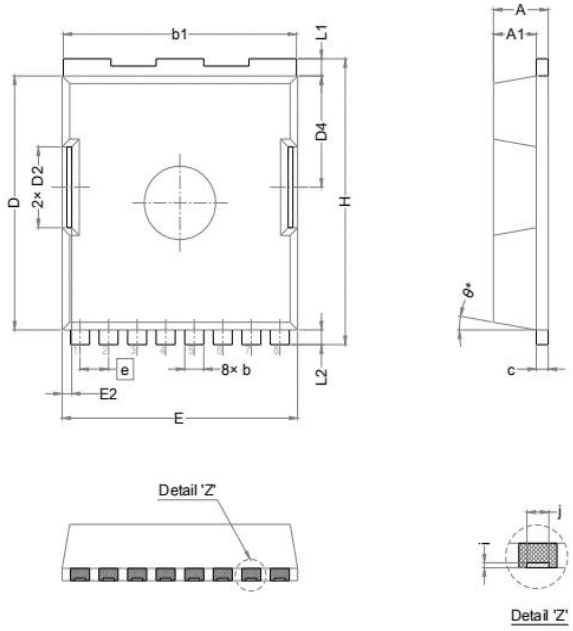
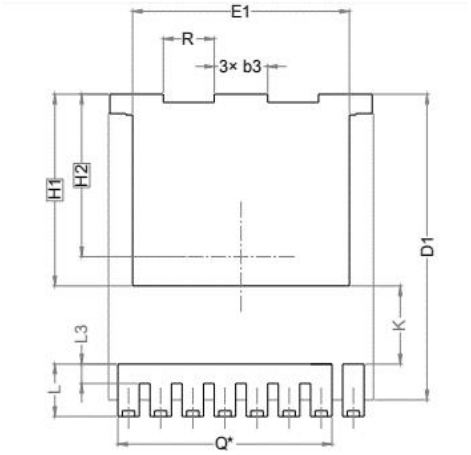


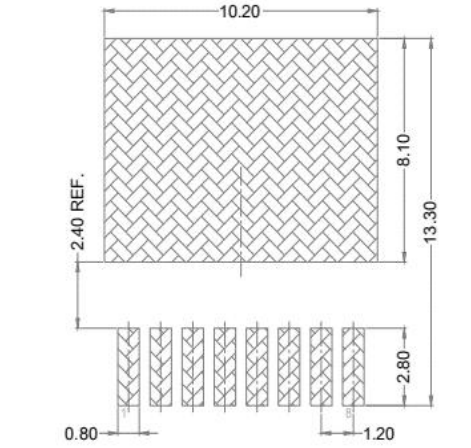
Fig.12 ID vs. Junction Temperature③



●TOLL Package Outline







SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.90	2.00	2.10
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.30	0.40	0.50
e	1.20 BSC		
H	11.58	11.68	11.78
H1	6.95 BSC		
H2	5.89 BSC		
i	0.10 REF.		
j	0.46 REF.		
K	2.80 REF.		
L	1.60	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.60	0.70	0.80
N	8		
Q	6.80 REF.		
R	1.80	1.90	2.00
θ	10° REF.		

Note:

① Pulse : VGS=+20V/-20V, Duty cycle=50%,Tj=175℃, t=1000 hours; For DC， the following test conditions can be passed: VGS=+20V/-10V, Tj=175℃, t=1000 hours；

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate；

③Practically the current will be limited by PCB, thermal design and operating temperature. VGS=10V.

Disclaimer

● Reproducing and modifying information of the document is prohibited without permission from ZMJ SEMICONDDUCTORS CO.,LTD.

● ZMJ SEMICONDDUCTORS CO.,LTD. reserves the rights to make changes of the content herein the document anytime without notification. Please refer to our website for the latest document.

● ZMJ SEMICONDDUCTORS CO.,LTD. disclaims any and all liability arising out of the application or use of any product including damages incidentally and consequentially occurred.

● ZMJ SEMICONDDUCTORS CO.,LTD. does not assume any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

● Applications shown on the herein document are examples of standard use and operation. Customers are responsible in comprehending the suitable use in particular applications. ZMJ SEMICONDDUCTORS CO.,LTD. makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

● The products shown herein are not designed and authorized for equipments relating to human life and for any applications concerning life-saving or life-sustaining, such as medical instruments, aerospace machinery et cetera. Customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify ZMJ SEMICONDDUCTORS CO.,LTD. for any damages resulting from such improper use or sale.

● Since ZMJ uses lot number as the tracking base, please provide the lot number for tracking when complaining.

Revision History

Version	Date	Change
A	2023.5.12	New
B	2024.4.16	Modified ciss,Qg,switch time